S&H Form: (02/05)

APPEAL BRIEF FEE TRANSMITTAL

Attorney Docket No.	1614.1109
Application Number	09/750,051
Filing Date	December 29, 2000
First Named Inventor	Shogo FUJIMORI et al.
Group Art Unit	2123
Examiner Name	Eduardo Garcia Otero

AMOUNT ENCLOSED	500.00

FEE CALCULATION (fees effective 12/08/04)

CLAIMS AS AMENDED	Claims Remaining After Amendment	Highest Number Previously Paid For	Number Extra	Rate	Calculations
TOTAL CLAIMS	22	- 22 =	0	X $ 50.00 =	$ 0.00
INDEPENDENT CLAIMS	3	- 3 =	0	X $ 200.00 =	0.00

Since an Official Action set an original due date of _, petition is hereby made for an extension to cover the date this reply is filed for which the requisite fee is enclosed (1 month ($120)); (2 months ($450)); (3 months ($1,020)); (4 months ($1,590)); (5 months ($2,160):	
If Appeal Brief is enclosed, add ($500.00)	500.00
If Statutory Disclaimer under Rule 20(d) is enclosed, add fee ($130.00)	
Information Disclosure Statement (Rule 1.17(p)) ($180.00)	
Total of above Calculations =	$ 500.00
Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28)	
TOTAL FEES DUE =	$ 500.00

(1) If entry (1) is less than entry (2), entry (3) is "0".
(2) If entry (2) is less than 20, change entry (2) to "20".
(4) If entry (4) is less than entry (5), entry (6) is "0".
(5) If entry (5) is less than 3, change entry (5) to "3".

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SUBMITTED BY: STAAS & HALSEY LLP

Typed Name	Paul W. Bobowiec	Reg. No.	47,431
Signature	Paul W. Bobowiec	Date	May 27, 2005

Docket No. 1614.1109

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shogo FUJIMORI et al.

Application No.: 09/750,051 Group Art Unit: 2123

Confirmation No. 7012

Filed: December 29, 2000 Examiner: Eduardo Garcia Otero

For: NOISE COUNTERMEASURE DETERMINATION METHOD AND APPARATUS AND STORAGE MEDIUM

APPEAL BRIEF UNDER 37 CFR §41.37

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In a Notice of Appeal filed March 28, 2005 (March 27, 2005 being a Sunday) the applicant appealed the Examiner's rejections of claims 1-22 asserted in the Advisory Action mailed March 14, 2005, the due date for filing of the Appellant's Brief being May 27, 2005. Appellant's Brief together with the requisite fee set forth in 37 CFR § 1.17 is submitted herewith.

I. REAL PARTY IN INTEREST (37 CFR § 41.37(c)(1)(i))

The real party in interest is Fujitsu Limited, the assignee of the subject application.

II. RELATED APPEALS AND INTERFERENCES (37 CFR § 41.37(c)(1)(ii))

The applicant and the undersigned representative are not aware of any other appeals or interferences that will directly affect or be directly affected by, or have a bearing on, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS (37 CFR § 41.37(c)(1)(iii))

Claim 1-22 are pending.

Claims 1-3, 7-12, and 16-22 stand rejected under 35 U.S.C. §102(b) as anticipated by Tsuchida (U.S.P. 5,559,997) and are on appeal; claims 4 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuchida in view of Dorf (The Electrical Engineering Handbook, Second Edition, Richard C. Dorf, Editor CRC Press, 1997) and are on appeal; and claims 5-6 and 14-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuchida in view of Guo (U.S.P. 6,597,808) and are on appeal.

IV. STATUS OF AMENDMENTS (37 CFR § 41.37(c)(1)(iv))

No amendments have been filed subsequent to the final rejection made on March 14, 2005.

V. SUMMARY OF INVENTION (37 CFR § 41.37(c)(1)(v))

Claim 1 recites a noise countermeasure determination method (FIG. 3, pages 14-15). The method of claim 1 includes calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis (step 3 illustrated in FIG. 3, pages 14-15). Claim 1 also recites a method comparing the input circuit information and the recommended circuit information (step 5 illustrated in FIG. 3, pages 14-15). Claim 1 also recites a method determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures (step 5 illustrated in FIG. 3, pages 14-15).

Claim 10 recites a noise countermeasure determination apparatus (FIG. 1, pages 12-13).

The apparatus of claim 10 includes a recommended circuit information calculating section calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis (step 3 illustrated in FIG. 4 and pages 15-17). The apparatus of claim 10 also includes a noise countermeasure determination section comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures (step 5 illustrated in FIG. 4 and pages 15-17).

Claim 19 recites a computer-readable storage storing a program for controlling a computer to determine noise countermeasures by calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis. (FIG. 1, pages 12, 13). Claim 19 also recites a computer-readable storage storing a program for controlling a computer to determine noise countermeasures by comparing the input circuit information and the recommended circuit information and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures (step 5 illustrated in FIG. 4 and pages 15-17).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 CFR § 41.37(c)(1)(vi))

Claims 1-3, 7-12, and 16-22 stand rejected under 35 U.S.C. §102(b) as anticipated by Tsuchida (U.S.P. 5,559,997); claims 4 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuchida in view of Dorf (The Electrical Engineering Handbook, Second Edition, Richard C. Dorf, Editor CRC Press, 1997); and claim 5 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuchida in view of Guo (U.S.P. 6,597,808).

FIG. 4 is objected to as not being functional.

VII. ARGUMENT OF EACH GROUND OF REJECTION PRESENTED FOR REVIEW (37 CFR § 41.37(c)(1)(vii))

All arguments are directed to the grounds of rejection. All citations to "Office Action" refer to the last and final Office Action mailed September 27, 2004, and all citations to "Advisory Action" refer to the last Advisory Action mailed March 14, 2005.

A. Claim 1

In page 5, items 27-28, the Examiner cites Tsuchida as providing these features. More specifically, the Examiner cites the Abstract and FIG. 1. As discussed below, Tsuchida does not discuss the features of claim 1 for which it is cited.

1. Features Not Discussed By Cited Art

To establish anticipation under §102, the prior art must teach each and every feature recited in the claim. See Manual Of Patent Examining Procedure § 2131 (8th ed. Rev. 2 May 2004)("MPEP"); *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Determining Noise Countermeasures Not Discussed in Tsuchida

Claim 1 recites a noise countermeasure determination method "comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures." (Emphasis added).

Instead, Tsuchida merely discusses (col. 3, starting at line 10):

> (t)he circuit board information indicates a board to be used for a circuit board to be designed, a circuit to be laid out on the board, and components to be included in the circuit. The noise reduction information indicating anti-noise solution, the evaluation information indicating electric characteristics of the circuit board in process of designing.

That is, Tsuchida does not teach how the "noise reduction components" (that is, noise countermeasures) are determined. Tsuchida merely relates to a method of designing a printed-circuit (PC) board based on fundamental circuit design and the "noise reduction components" (that is, noise countermeasures) that are input.

Hence, Tsuchida does not calculate recommended circuit information, and does not compare the input circuit information and the recommended circuit information, so as to determine the "noise reduction components" (that is, noise countermeasures). In other words, Tsuchida merely determines whether to insert a noise reduction component within a limited range based on a predetermined rule, and does not teach how the "noise reduction components" (that is, noise countermeasures) may be determined.

The Examiner refers to element 2103 in Fig. 1 of Tsuchida and the looping path through

2103, 2104, 2105, 2106, 2107, 2109 and 2103 as teaching how the "noise reduction components" (that is, noise countermeasures) may be determined.

However, the looping path of Tsuchida merely corresponds to a general PC board design procedure. Tsuchida teaches (col. 1, lines 15-53):

> the designer designs an electric circuit showing the electric connection among all the components to be mounted on the printed circuit board, with the use of CAD for circuits (step 2101). To be more specific, the designer designs a fundamental electric circuit (step 2102), and adds noise reduction components which are necessary for preventing reflection, delay, and noise (step 2103). . . it may be found that the PC board does not work properly or cannot put out expected performance due to electric characteristics such as signal delay, noise, . . the designer modifies the rated value, such as the resistance value or capacity value of each noise reduction component (step 2108) . . . In the case that the PC board still does not work properly or cannot put out expected performance, the layout including the placement of components and routing foils or route length is modified (step 2104), and it is examined whether the board works properly as is expected (steps 2105, 2106, 2107, and 2109). If the PC board still does not work properly or cannot put out expected performance, additional noise reduction components such as a resistance or capacitor are provided (step 2103).

That is, Tsuchida merely teaches that if the PC board does not work properly or cannot put out expected performance due to electric characteristics such as signal delay, noise or electromagnetic radiation, a rated value, such as the resistance value or capacity value of each noise reduction component, is modified and examined through a simulation whether the PC board operates as is expected.

In the general PC board design procedure (looping path) as taught in Tsuchida the modification of the rated value of each noise component and the simulation are repeated until the PC board performance is optimized to the expected performance. In other words, Tsuchida teaches simply modifies the rated value of each noise reduction component manually to optimize the PC board performance.

Tsuchida does not teach determining noise countermeasures based on the input circuit information that is input

Rather Tsuchida requires modified "noise reduction components" (that is, noise countermeasures) to be input in order to optimize the PC board performance.

Tsuchida does not calculate a recommended circuit information that is considered to minimize a noise by use of at least one formula based on input circuit information amounting to

at least one net of a target circuit which is to be subjected to a noise analysis, and compares the input circuit information and the recommended circuit information, so as to determine the noise countermeasures by determining a differing portion of the recommended circuit information differing from the input circuit information.

Tsuchida merely modifies a rated value of each noise reduction component manually until the expected PC board performance is obtained.

Thus, the rejection is incorrect since none of the cited art discusses features recited by claim 1.

B: Claims 2-3, 7-9, and 20-22

As discussed above with reference to claim 1, Tsuchida does not discuss comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

Claims 2-3, 7-9, and 20-22 more specifically recite a noise countermeasure determination method, or features thereof. Claim 2 recites a noise countermeasure determination method "further comprising: creating a simulation model of the input circuit information after determining the noise countermeasures; carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and categorizing the noise existing as a result of the noise check, and optimizing the determined noise countermeasures to only portions related to the noise."

Claim 3 recites a noise countermeasure determination "wherein the calculating recommended circuit information comprises outputting a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage VIH-2 which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range."

Claim 7 recites a noise countermeasure determination method "further comprising:

creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform; and categorizing the noise existing as a result of the noise check and optimizing the determined noise countermeasures to only portions related to the noise."

Claim 8 recites a noise countermeasure determination method "wherein said creating a simulation model creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween."

Claim 9 recites a noise countermeasure determination method "wherein said creating a simulation model and said carrying out a circuit simulation using the simulation model are repeated while changing the pattern gap, so as to obtain a minimum pattern gap with which the noise obtained as a result of the noise check carried out in said carrying out a circuit simulation using the simulation model does not exceed the tolerable range, and said comparing the input circuit information and the recommended circuit information determines the minimum pattern gap as the noise countermeasures."

Claim 20 recites a noise countermeasure determination method "further comprising carrying out at least one of a circuit rule check and a wiring topology check with respect to the input circuit information." Claim 21 recites a noise countermeasure determination method "further comprising outputting an advice based on a check result obtained." Claim 22 recites a noise countermeasure determination method "further comprising correcting the input circuit information based on the advice output."

As discussed above with reference to claim 1, the rejection is incorrect since none of the cited art teach features recited by claims 2-3, 7-9, and 20-22 further defining the method recited by claim 1.

C. Claim 10

Claim 10 is patentable over the cited art, for reasons similar to those discussed above for claim 1. Claim 10 is similar to claim 1, but specifies a noise countermeasure determination

apparatus including "a noise countermeasure determination section comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures."

As discussed above with reference to claim 1, the rejection is incorrect since none of the cited art discusses each feature recited in claim 1 including comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

D. Claims 11-12 and 16-18

As discussed above with reference to claim 10, Tsuchida does not discuss comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

Claims 11-12 and 16-18 more specifically recite a noise countermeasure determination apparatus, or the features thereof.

Claim 11 recites a noise countermeasure determination apparatus "further comprising: a circuit model creating section creating a simulation model of the input circuit information after determining the noise countermeasures in said noise countermeasure determination section; a simulation and check section carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and a noise countermeasure optimizing section categorizing the noise existing as a result of the noise check carried out in said simulation and check section, and optimizing the determined noise countermeasures to only portions related to the noise."

Claim 12 further recites a noise countermeasure determination apparatus "wherein said recommended circuit information calculating section outputs a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage VIH-2 which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a

damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range."

Claim 16 recites a noise countermeasure determination apparatus "further comprising: a circuit model creating section creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures by said noise countermeasure determination section; a simulation and check section carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform; and a noise countermeasure optimizing section categorizing the noise existing as a result of the noise check carried out by said simulation and check section, and optimizing the determined noise countermeasures to only portions related to the noise.

Claim 17 recites a "noise countermeasure determination apparatus as claimed in claim 16, wherein said circuit model creating section creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween."

Claim 18 recites a noise countermeasure determination apparatus "wherein processes of said circuit model creating section and said simulation and check section are repeated while changing the pattern gap, so as to obtain a minimum pattern gap with which the noise obtained as a result of the noise check carried out by said simulation and check section does not exceed the tolerable range, and said noise countermeasure determination section determines the minimum pattern gap as the noise countermeasures."

As discussed above with reference to claim 10, the rejection is incorrect since none of the cited art teach features recited by claims 11-12 and 16-18 further defining the apparatus recited by claim 10.

E. Claim 4

In page 9, items 56-57 of the Action, the Examiner acknowledges that Tsuchida does not teach a method:

comprising a damping resistance which makes a voltage at a time of a ringback

> equal to the minimum voltage VIH-1 and the minimum value of the damping resistance, and outputs(ing) a larger one of the damping resistance.

Dorf is cited as providing these features. More specifically the Examiner cites page 2271 equation (110.27) "undershoot" for transient responses and FIG. 100.6.

1. Features Not Discussed By Cited Art

To establish obviousness under §103, the Examiner must consider the claimed invention "as a whole," and the prior art must teach or suggest all of the claim features. *See* Manual Of Patent Examining Procedure § 2143.03 (8th ed. Rev. 2 May 2004)("MPEP"); *In re Royka*, 180 U.S.P.Q. 580, 583 (C.C.P.A. 1974); *In re Fine*, 5 U.S.P.Q.2d 1596, 1599 (Fed. Cir. 1988); *Ruiz v. A.B. Chance Co.*, 69 U.S.P.Q.2d 1686, 1690 (Fed. Cir. 2004).

Comparing Damping Resistance Not Discussed In Dorf

Claim 4 recites a noise countermeasure determination method "wherein the calculating recommended circuit information comprises: comparing a damping resistance which makes a voltage at a time of a ringback equal to the minimum voltage VIH-1 and the minimum value of the damping resistance, and outputting a larger one of the compared values as the minimum value of the damping resistance."

Dorf does not discuss the features in the lines cited by the Examiner, or anywhere else.

Thus, the rejection is incorrect since none of the cited art discusses features recited by clam 4.

2. Improper Combination

Further, the basis for combining the prior art references of Tsuchida and Dorf is the assumption that Tsuchida "implicitly teaches towards the importance of staying above the minimum voltage during the undershoot." (Action at page 9, item 58).

In page 3, item 16 of the Action the Examiner contends that since Tsuchida discusses an "allowable range" of voltage for overshoot Tsuchida "implicitly teaches towards the importance of staying over the minimum voltage during the undershoot."

As set forth in MPEP 2144.04:

> (t)he mere fact that worker in the art could rearrange the parts of the reference . . . is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's

> specification, to make the necessary changes in the reference device. *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).

It is understood in the art that a teaching to remain within a range for one type of voltage response, does not implicitly teach a desire for modification for remaining within a range for another type and different type of response.

That is, there is no implicit teaching in Tsuchida as the Examiner contends.

Thus, the Examiner's contention that it is obvious to modify Tsuchida is not valid and the rejection is incorrect.

F. Claim 13

Claim 13 is patentable over the cited art, for reasons similar to those discussed above for claim 4.

Claim 13 is similar to claim 4, but specifies a noise countermeasure determination apparatus "wherein said recommended circuit information calculating section compares a damping resistance which makes a voltage at a time of a ringback equal to the minimum voltage VIH-1 and the minimum value of the damping resistance, and outputs a larger one of the compared values as the minimum value of the damping resistance."

As discussed above with reference to claim 4, the rejection is incorrect since features recited by claim 13 are not taught by the cited art, alone or in combination, and there is no motivation to combine the art.

G. Claims 5 and 14

Claim 5 recites a noise countermeasure determination method "further comprising outputting input circuit information that includes a wiring length that is substantially a Manhattan distance that is determined based on positions of part pins forming the target circuit and a wiring topology."

Claim 14 is similar to claim 5 , but specifies a noise countermeasure determination apparatus.

In page 9, items 56-57, the Examiner acknowledges that Tsuchida does not teach a method:

> . . . outputting the input circuit information which includes as, a wiring length, a Manhattan distance which is determined based on positions of part pins forming the

target circuit and a wiring topology.

Guo is cited as teaching this feature.

To establish a *prima facie* case of obviousness based on multiple references, there must be some teaching that would have led one of ordinary skill in the art at the time of the invention to combine the references. MPEP § 2143.01; *In re Thrift*, 63 U.S.P.Q. 2d 2002, 2006 (Fed. Cir. 2002)(quoting *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988)); *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

The Examiner contends that is obvious to modify Guo since:

> (o)ne of ordinary skill in the art would have started with Tsuchida . . . as disclosing an "allowable range" of voltage for the overshoot, and then looked to Guo for common techniques of characterizing distance between points.

Applicants there is no teaching in Tsuchida to support a modification as the Examiner contends and the Examiner has not supported his contention, as set forth in MPEP 2144.04, for modification of Tsuchida of an "allowable range" to a determination by a Manhattan distance.

Since *prima facie* obviousness is not established, the rejection of claims 5 and 14 is incorrect.

H. Claim 6 and 15

Claim 6 recites a noise countermeasure determination method "further comprising: creating a simulation model of the input circuit information after determining the noise countermeasures; carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and repeating the creating a simulation model and the carrying out a circuit simulation using the simulation model using a plurality of wiring topologies, and determining an optimum wiring topology from results of the noise check carried out in said carrying out a circuit simulation using the simulation model to use in said, outputting input circuit information so that the optimum wiring topology is determined as the noise countermeasures in said comparing the input circuit information and the recommended circuit information." (Emphasis added).

Claim 15 is similar to claim 6 but recites a noise countermeasure apparatus.

In item 18, page 4 of the Action, the Examiner contends that Tsuchida FIG. 1 teaches an "optimum wiring topology" since Tsuchida FIG. 1 is an "optimizing iterative loop."

As provided in MPEP §2143.03 "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F. 2d 1981, (CCPA 1974)."The cited art, alone or in combination, does not teach an optimum wiring topology.

Tsuchida merely teaches a replacement of components and "changeable parts" (Step 2109 FIG. 1). Not a "optimum wiring topology."

Since *prima facie* obviousness is not established, the rejection of claims 6 and 15 is incorrect.

I. FIG. 4

FIG. 4 illustrates (pages 15, starting at line 12) "in this second embodiment, the noise countermeasures determined by the first embodiment are further optimized."

FIG. 4 clearly, sufficiently and correctly shows features according to an aspect of a first embodiment of the present *invention*, and the description in the specification related to FIG. 4 is clear and sufficient to enable those skilled in the art to understand the subject matter of the present invention recited in claims 1-22.

In the Advisory Action page 2, the Examiner contends:

> FIG. 4 does not appear to have feedback/optimizing loop as discussed in the clams. Rather, FIG. 4 appears to have some kind of feedforward loop, which branches from element 5 to elements 6 or element 7. This type of feedforward branching is generally displayed by a diamond that indicates the type of branching decision which decides which path to follow. FIG. 4 does not appear to have a feedback loop which is typical of optimization procedures. In view of the specification and the claims, FIG. 4 does not appear to be functional, and certainly does not follow standard flow diagram conventions for illustrating branching.

As described in the specification (page 14, line 7 to page 17, line 10), step 3 calculates the recommended circuit information that is considered to minimize the noise using at least one calculation formula, based *on* the input circuit information read from the memory part 202. Step 5 compares the input circuit information, and the recommended circuit information, and determines the differing portions of the recommended circuit information as the noise countermeasures, and step 6 outputs the determined noise countermeasures by displaying the

noise countermeasures on the display 102, for example.

Step 9 performs a noise check by detecting the noise existing in a signal waveform propagating through a wiring of the electronic circuit, for example, which signal waveform is output from the circuit simulator. Step 10 categorizes results of the noise check (step 9), and restricts the noise countermeasures output by the step 6 to only portions related to the categorized results of the noise check.

Hence, step 11 can output the restricted noise countermeasures by displaying the restricted noise countermeasures on the display 102, for example.

Accordingly, a "feedback/optimization loop" for optimizing the "PC board performance" such as taught by Tsuchida is not illustrated in FIG. 4, since the present invention does not relate to optimization of the PC board performance.

When optimizing the PC board performance, the PC board performance may be optimized using the noise countermeasures that are obtained by step 6 shown in FIG. 3 in the case of the first embodiment or, using the optimized noise countermeasures that are obtained by step 11 shown in FIG. 4 in the case of the second embodiment, for example. As understood in the art, this does preclude a "feedback/optimization loop" within any of the steps 8-10.

In addition, step 10 categorizes results of the noise check (step 9), and restricts the noise countermeasures output by step 6 to only portions related to the categorized results of the noise check, so as to optimize the noise countermeasures as shown in FIG. 4.

For this reason, the arrow from step 6 towards step 10 is required in FIG. 4 in order to illustrate an optimization of the noise countermeasures, contrary to the Examiner's assertion. Hence, the optimization of the "noise countermeasures" is correctly illustrated in FIG. 4 and clearly and sufficiently described in the specification.

With regard to the Examiner's assertion that "FIG. 4 does not appear to have a feedback/optimizing loop as discussed in claims," the optimization of the "noise countermeasures" is recited in claims 2, 7, 11 and 16, and the related operations 5-11 are clearly illustrated in FIG. 4 and described in the specification for the second embodiment, for example.

Thus, FIG. 4 is correct, and the objection to FIG. 4 is not valid. Moreover, the changes proposed by the Examiner would not conform to the original disclosure in the specification and the recited claims.

VI. CONCLUSION

In summary, Applicants submits that all pending claims 1-22 patentably distinguish over the prior art. Reversal of the Examiner's rejection is respectfully requested.

Respectfully submitted,

STAAS & HALSEY LLP

Date: May 27, 2005

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CLAIMS APPENDIX (37 CFR § 41.37(c)(1)(viii))

1. (PREVIOUSLY PRESENTED) A noise countermeasure determination method comprising:

calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and

comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

2. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, further comprising:

creating a simulation model of the input circuit information after determining the noise countermeasures;

carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and

categorizing the noise existing as a result of the noise check, and optimizing the determined noise countermeasures to only portions related to the noise.

3. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, wherein the calculating recommended circuit information comprises outputting a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage VIH-2 which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range.

4. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 3, wherein the calculating recommended circuit information comprises:

comparing a damping resistance which makes a voltage at a time of a ringback equal to

the minimum voltage VIH-1 and the minimum value of the damping

resistance, and

outputting a larger one of the compared values as the minimum value of the damping resistance.

5. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, further comprising outputting input circuit information that includes a wiring length that is substantially a Manhattan distance that is determined based on positions of part pins forming the target circuit and a wiring topology.

6. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 5, further comprising:

creating a simulation model of the input circuit information after determining the noise countermeasures;

carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and

repeating the creating a simulation model and the carrying out a circuit simulation using the simulation model using a plurality of wiring topologies, and determining an optimum wiring topology from results of the noise check carried out in said carrying out a circuit simulation using the simulation model to use in said, outputting input circuit information so that the optimum wiring topology is determined as the noise countermeasures in said comparing the input circuit information and the recommended circuit information.

7. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, further comprising:

creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures

carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform; and

categorizing the noise existing as a result of the noise check

and optimizing the determined noise countermeasures to only portions related to the noise.

8. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 7, wherein said creating a simulation model creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween.

9. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 8, wherein said creating a simulation model and said carrying out a circuit simulation using the simulation model are repeated while changing the pattern gap, so as to obtain a minimum pattern gap with which the noise obtained as a result of the noise check carried out in said carrying out a circuit simulation using the simulation model

does not exceed the tolerable range, and said comparing the input circuit information and the recommended circuit information determines the minimum pattern gap as the noise countermeasures.

10. (ORIGINAL) A noise countermeasure determination apparatus comprising:

a recommended circuit information calculating section calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and

a noise countermeasure determination section comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

11. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 10, further comprising:

a circuit model creating section creating a simulation model of the input circuit information after determining the noise countermeasures in said noise countermeasure determination section;

a simulation and check section carrying out a circuit simulation using the simulation

model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and a noise countermeasure optimizing section categorizing the noise existing as a result of the noise check carried out in said simulation and check section, and optimizing the determined noise countermeasures to only portions related to the noise.

12. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 10, wherein said recommended circuit information calculating section outputs a range of a damping resistance as the recommended circuit information, based on a minimum voltage VIH-1 and a maximum voltage VIH-2 which guarantee a normal operation of the target circuit, by taking a damping resistance which makes a first rising voltage of an input waveform at a receiving end of the target circuit equal to the minimum voltage VIH-1 as a maximum value of the range, and taking a damping resistance which makes the first rising voltage of the input waveform at the receiving end of the target circuit equal to the maximum voltage VIH-2 as a minimum value of the range.

13. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 12, wherein said recommended circuit information calculating section compares a damping resistance which makes a voltage at a time of a ringback equal to the minimum voltage VIH-1 and the minimum value of the damping resistance, and outputs a larger one of the compared values as the minimum value of the damping resistance.

14. (PREVIOUSLY PRESENTED) The noise countermeasure determination apparatus as claimed in claim 10, further comprising:

a circuit information output section outputting input circuit information that includes a wiring length that is substantially a Manhattan distance that is determined based on positions of part pins forming the target circuit and a wiring topology.

15. (PREVIOUSLY PRESENTED) The noise countermeasure determination apparatus as claimed in claim 13, further comprising:

a circuit model creating section creating a simulation model of the input circuit information after determining the noise countermeasures in said noise countermeasure determination section; and

a simulation and check section carrying out a circuit simulation using the simulation

model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform

wherein processes of said circuit model creating section and said simulation and check section being repeated using a plurality of wiring topologies, and an optimum wiring topology being determined from results of the noise check carried out by said simulation and check section for use by said circuit model creating section, so that the optimum wiring topology is determined as the noise countermeasures by said noise countermeasure determination section.

16. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 10, further comprising:

a circuit model creating section creating a simulation model of input circuit information made up of circuit information of a target net which is to be subjected to the noise analysis and circuit information of an adjacent net which is adjacent to the target net, after determining the noise countermeasures by said noise countermeasure determination section;

a simulation and check section carrying out a circuit simulation using the simulation model, to obtain a noise combined waveform by combining a crosstalk noise waveform and a signal waveform propagating through the target net which are calculated, and to check whether or not a noise exceeding a tolerable range exists based on the noise combined waveform; and

a noise countermeasure optimizing section categorizing the noise existing as a result of the noise check carried out by said simulation and check section, and optimizing the determined noise countermeasures to only portions related to the noise.

17. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 16, wherein said circuit model creating section creates the simulation model by assuming that the circuit information of the adjacent net is related to a net which has the same structure as the target net and is adjacent to the target net with a constant pattern gap formed therebetween.

18. (ORIGINAL) The noise countermeasure determination apparatus as claimed in claim 17,

wherein processes of said circuit model creating section and said simulation and check section are repeated while changing the pattern gap, so as to obtain a minimum pattern gap with which the noise obtained as a result of the noise check carried out by said simulation and check section does not exceed the tolerable range, and said noise countermeasure determination section determines the minimum pattern gap as the noise countermeasures.

19. (PREVIOUSLY PRESENTED) A computer-readable storage storing a program for controlling a computer to determine noise countermeasures, by:

calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and

comparing the input circuit information and the recommended circuit information and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures.

20. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 1, further comprising carrying out at least one of a circuit rule check and a wiring topology check with respect to the input circuit information.

21. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 20, further comprising outputting an advice based on a check result obtained.

22. (PREVIOUSLY PRESENTED) The noise countermeasure determination method as claimed in claim 21, further comprising correcting the input circuit information based on the advice output.